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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/767,830	YAMADA ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondenc address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *335-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,28,29 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 36-40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7

Specification

The substitute specification filed 7/30/2001 and amendments filed 12/16/2002 have been entered.

The disclosure is objected to because of the following informalities:

In line 2 of paragraph [0028], "seqnd" should be replaced with --second--.

In line 2 of paragraph [0110], "rdade" should be replaced with –made--.

In line 5 of paragraph [0119], "si" should be replaced with –is--.

In line 12 of paragraph [0136], "prefe rable" should be replaced with --preferable--

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-29 and 34-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claim 34-35, it is not clear to the examiner what is meant by "forming second semiconductor regions in said semiconductor substrate through an impurity diffusion from said conductive film an of forming said source and drain regions of said first and second semiconductor regions" in lines 26-30. The language is unclear as to how the second semiconductor regions are formed.

Furthermore, in re claims 28-29 and 34- 35, after carefully reviewing th4 figures and the specification of the elected first embodiment it is evident that there are numerous different insulating layers an it is not clear which of the insulating layers are the first and second insulating layers that are referred to in claim 34. The examiner requests that Applicant's reply to this rejection includes a specific Figure and reference numerals clearly indicating which insulating layers are the first and second insulating layers as defined in claims 28 and 34.

Claims 28-29 and 34-35 will be examined as best understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 4-7 rejected under 35 U.S.C. 102(b) as being anticipated by Baba et al. (U.S. Patent No. 5,733,810).

Baba discloses the method of forming a semiconductor integrated circuit device, at the time of forming field effect transistors in a semiconductor substrate; comprising the steps of: (a) forming trenches (4) in said semiconductor substrate; (b) forming a gate insulating film (5) inside of said trenches; (c) forming gate electrodes (6) which are completely or partially, buried within said trenches under the condition where said gate insulating film is interposed between said gate electrodes and said semiconductor substrate within said trenches; and (d) forming semiconductor regions for the sources and drains (7) wherein in said semiconductor substrates wherein said Step (a) contains the step of rounding the bottom corners within said trenches so that the sub-threshold coefficient of said field effect transistors does not exceed a predetermined value, and said Step (b) contains the step of forming said forming a gate insulating film inside of gate insulating film through a deposition method (see column 6, lines 25-54 and column 8, lines 10-29).

Baba et al. further discloses the method wherein said Step (a) contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy (see column 4, lines 20-35) and wherein said Step (b) contains the step of forming part of said gate insulating film by oxidizing the inner walls of said trenches and wherein the radius of curvature of the bottom corners within said trenches is 10 nm or more (see column 6, lines 24-31).

Claims 33-35 are is rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al. (U.S. Patent No. 5,177,576).

In re claim 33, Kimura et al. discloses the method of forming a semiconductor integrated comprising the steps of: forming element isolation parts (9, see column 6, lines 28-40) in a semiconductor substrate; forming a mask (2) having apertures over said semiconductor substrate; forming first trench in the semiconductor substrate which has been exposed from said apertures; (d) forming a first film (11) in said first trench; (e) removing part of said first film (see Figure 6 J) so that part of said and first film remains in said first trench; forming a second film (15) so as to fill in recesses on the surface of said first film.

In re claims 34-35, Kimura discloses the method of forming a semiconductor integrated circuit device which has a plurality of memory cells having field effect transistors with buried gate electrodes (28) formed semiconductor substrate (10) and capacitor elements electrically connected to at least one of the source or drain regions of said field effect transistors are provided, comprising the steps of: forming first semiconductor regions in said semiconductor substrate; (b) forming a first trench in said semiconductor substrate; forming a gate insulating film (26), gate electrodes (28) and a first insulating film (8) of silicon nitride inside said first trench; forming a second insulating film (9) of silicon oxide on the semiconductor substrate and, further on said first insulating film; forming apertures (see Figure 6G), in said second insulating film, which overlap said first semiconductor regions in a plane manner through a method where the etching rate of said second insulating film is faster than the etching rate of the

first insulating film; forming a conductive film (11) inside of said apertures, and forming second semiconductor regions said semiconductor substrate through an impurity diffusion from said conductive film and of forming said source insulating film; conductive film inside of said and drain regions of said first and second semiconductor regions (see column 6, lines 35-50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 6,200,855) in view of Baba et a. (U.S. Patent No. 5,733,810).

Lee discloses the method of forming a semiconductor integrated circuit device where a plurality of memory cells which have field effect transistors formed in a semiconductor substrate and capacitor elements connected to the source and drain regions of said field effect transistors are provided.

Lee does not disclose the method of utilizing a buried gate transistor including the steps of forming trenches of which the radius of curvature of the bottom corners is larger than 10 nm in said semiconductor substrate; forming a first gate insulating film through a deposition method inside of said trenches; and forming gate electrodes within said trenches and placing said gate electrodes on said first gate insulating film and

including a step of forming a second gate insulating film by oxidizing the inner walls of said trenches and wherein forming said trenches contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy.

Baba et al. discloses the method of forming trenches of which the radius of curvature of the bottom corners is larger than 10 nm in said semiconductor substrate; forming a first gate insulating film through a deposition method inside of said trenches; and forming gate electrodes within said trenches and placing said gate electrodes on said first gate insulating film and including a step of forming a second gate insulating film by oxidizing the inner walls of said trenches and wherein forming said trenches contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy (see columns 4, lines 20-35, column 6, lines 25-55 and column 8, lines 10-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Lee et al. by the method of Baba et al. since the method Baba et al. allows for a gate that is buried (vertical) such that there is an ease in forming a short channel length transistor without severe lithography constraints as in the fabrication of the short channel length planar transistor and further

there are lower production costs owing to the planar process featured by the use of a flat main surface of a semiconductor wafer.

Allowable Subject Matter

Claims 8-27 and 30-32 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, singly or in combination, fails to anticipate or render obvious, the method, including the limitations of forming a mask which has apertures crossing over the element isolation parts, forming a second trench in the element isolation parts which have been exposed through the apertures, forming a third trench in the semiconductor substrate which has been exposed through the apertures and the second trench and forming wires in the second and third trenches in combination with the other limitations of independent claims 8, 10, or 17.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmk

John F. Niebling
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